Designing with the AMD UltraScale™ and UltraScale+™ Families

2 days - 14 hours

OBJECTIVES

- After completing this training, you will have the necessary skills to:
  - 1- Describe the new CLB capabilities and the impact that they make on your HDL coding style
  - 2- Define the block RAM, FIFO, UltraRAM, and DSP resources available
  - 3 - Properly design for the I/O and SERDES resources
  - 4 - Identify the MMCM, PLL, and clock routing resources included
  - 5 - Describe the additional features of the dedicated transceivers
  - 6 - Effectively migrate your IP and design to the UltraScale architecture as quickly as possible

PREREQUISITES

- Basic knowledge FPGAs architectures
- A successful first experience of designing an VHDL–based FPGA using Vivado™ Design Suite

CONCERNED PUBLIC

- Technicians and Engineers in Digital Electronics
- All our training courses are given at a distance and are accessible to people with reduced mobility.
- Our partner AGEFIPH accompanies us to implement the necessary adaptations related to your disability.

NOTES

- Release date: 20/12/2021

CHAPTERS

DAY 1

- Objective 1
  - Introduction to the UltraScale Architecture {Lecture}
  - Introduction to the UltraScale+ Families {Lecture}
  - CLB Resources {Lecture, Lab}
  - HDL Coding Techniques {Lecture, Lab}
- Objective 2
  - Block RAM Memory Resources {Lecture}
  - FIFO Memory Resources {Lecture}
  - UltraRAM Memory Resources {Lecture, Lab}
  - HBM Memory Resources {Lecture}
  - DSP Resources {Lecture, Lab}

DAY 2

- Objective 3
  - UltraScale Architecture I/O Resources Overview {Lecture}
  - I/O Resources – Component Mode {Lecture, Lab}
  - I/O Resources – Native Mode {Lecture, Lab}
- Objective 4
  - Clocking Resources {Lectures, Lab}
- Objective 5
  - Architecture Transceivers {Lecture}
  - Transceivers Wizard {Lecture, Lab}
- Objective 6
  - FPGA Design Migration {Lecture, Labs}

TEACHING METHODS

- Inter-company online training :
  - Presentation by Webex by Cisco
  - Provision of course material in PDF format
  - Labs on Cloud PC by RealVNC

METHODS OF MONITORING AND ASSESSMENT OF RESULTS

- Attendance sheet
- Evaluation questionnaire
- Evaluation sheet on:
  - Technical questionnaire
  - Result of the Practical Works
  - Validation of Objectives
- Presentation of a certificate with assessment of prior learning

SUPPORT

- Authorized Trainer Provider AMD : Engineer Electronics and Telecommunications ENSIL
  - Expert AMD FPGA - Language VHDL/Verilog - RTL Design
  - Expert AMD SoC & MPSoC - Language C/C++ - System Design
  - Expert DSP & AMD RFSoC – HLS - Matlab - Design DSP RF
  - Expert AMD Versal – AI Engines – Heteregenous System Architect

PC RECOMMENDED

- Software Configuration :
  - WebEx Cisco
  - RealVNC Viewer
  - Vivado Design Suite 2021.1
- Hardware configuration:
  - Recent computer (i5 or i7)
  - OS Linux 64-bits (Windows 10 compatible)
  - At least 16GB RAM
  - Display resolution recommended 1920x1080

PARTNERS

AMD
Authorized Training Provider

CONTACT

Administratif / Formateur : (+33) 06 74 52 37 89
info@mvd-training.com

Qualiopi processus certifié
RÉPUBLIQUE FRANÇAISE
La certification a été délivrée au titre de la catégorie d'action suivante :
ACTIONS DE FORMATION